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Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended) A simultaneous bi-directional signal transmission system comprising a first semiconductor device, a second semiconductor device, and at least one transmission line which connects the first and second semiconductor devices,
 - wherein the first semiconductor device includes:
 - a first output MUX which receives a first binary data and converts the first binary data into a first signal having one of at least four levels;
 - a first transmitter which is connected to the first output MUX and outputs the first signal via the transmission line to the second semiconductor device;
 - a first receiver which compares at least one reference voltage selected by the first signal with a third signal input via the transmission line and outputs the comparison result; and
 - a first input encoder which detects a second binary data based on the comparison result output from the first receiver, and
 - wherein the second semiconductor device includes:
 - a second output MUX which receives the second binary data and converts the second binary data into a second signal having one of at least four levels;
 - a second transmitter which is connected to the second output MUX and outputs the second signal via the transmission line to the first semiconductor device;
 - a second receiver which compares at least one reference voltage selected by the second signal with the third signal input via the transmission line and outputs the comparison result; and
 - a second input encoder which detects the first binary data based on the comparison result output from the second receiver.

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2. (original) The system as claimed in claim 1, wherein the third signal is determined by a voltage level of the output first signal of the first transmitter and a voltage level of the output second signal of the second transmitter.

3. (original) The system as claimed in claim 1, wherein the third signal level is a signal having one of 7 levels.

4. (original) The system as claimed in claim 3, wherein the reference voltage is a voltage between one of the seven levels and one of the four levels.

5. (original) The system as claimed in claim 1, wherein the first transmitter includes an output driver and an impedance calibration circuit,

wherein the impedance calibration circuit performs calibration when the first semiconductor device is initialized and outputs an N-bit control signal for matching the impedance of the output driver connected to the transmission line with the impedance of the transmission line,

and wherein the output driver calibrates its own impedance in response to the N-bit control signal and drives the first signal to the transmission line in response to the first binary data and a logic value corresponding to the first signal.

6. (original) The system as claimed in claim 1, wherein the second transmitter includes an output driver and an impedance circuit,

wherein the impedance calibration circuit performs calibration when the second semiconductor device is initialized and outputs an N-bit control signal for matching the impedance of the output driver connected to the transmission line with the impedance of the transmission line,

and wherein the output driver calibrates its own impedance in response to the N-bit control signal, and drives the second signal to the transmission in response to the second binary data and a logic value corresponding to the second signal.

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7. (original) The system as claimed in claim 1, wherein the first receiver includes:
a reference voltage generator which generates a plurality of reference voltages; and
a comparison circuit which selects a reference voltage from the plurality of reference voltages in response to the first signal, compares the selected reference voltage with the third signal, and outputs the comparison result.

8. (original) The system as claimed in claim 7, wherein the second receiver includes:
a reference voltage generator which generates a plurality of reference voltages; and
a comparison circuit which selects a reference voltage from the plurality of reference voltages in response to the second signal, compares the selected reference voltage with the third signal, and outputs the comparison result.

9. (original) A semiconductor device comprising:
a pad;
an output MUX which receives a first binary data, converts the first binary data into an output signal having one of at least four levels;
a transmitter which is connected between the output MUX and the pad and drives the output signal via a transmission line, connected to the pad, to a signal transmission circuit;
a receiver which compares one or more reference voltages selected by the output signal with a signal received via the pad and outputs the comparison result; and
an input encoder which detects a second binary data output by the signal transmission circuit based on the comparison result of the receiver.

10. (original) The semiconductor device as claimed in claim 9, wherein the transmitter includes an output driver and an impedance calibration circuit,
wherein the impedance calibration circuit performs calibration when the semiconductor device is initialized and outputs an N-bit control signal for matching the impedance of the output driver connected to the transmission line to the impedance of the transmission line,

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and wherein the output driver calibrates the impedance of the output driver in response to the N-bit control signal and drives the output signal to the transmission line in response to the first binary data and a logic value corresponding to the first signal.

11. (original) The semiconductor device as claimed in claim 10, wherein the impedance calibration circuit includes:

a comparator which includes a first input terminal, a second input terminal, and an output terminal, compares a voltage of the first input terminal with the reference voltage input to the second input terminal, and outputs the comparison result,

a counter control circuit which is connected to the output terminal of the comparator and outputs a control signal based on the comparison result,

a counter which is connected to the counter control circuit and outputs the N-bit control signals that are up-count; and

a plurality of transistors, each of which is connected to a power supply voltage and the first input terminal of the comparator,

wherein each of the plurality of transistors is controlled in response to respective bits of the N-bit control signal,

and wherein the counter controls to hold a count value of the N-bit control signal in response to the control signal generated when the voltage of the first input terminal is equal to the reference voltage.